REMARKS

Claims 8-13 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention because claims 8-13 recite the limitation "device". There is insufficient antecedent basis for this limitation in the claim. For purpose of examination the "device" will be construed as the "microprocessor system" of claim 7.

Applicant has amended claims 8-13 to change the indefinite word "device" to the definite term "microprocessor system" as suggested by the Examiner. No new matter is entered.

Claims 1-13 are rejected under 25 USC 102b as being anticipated by Kaiser et al (US Patent No. 5,784,710).

Applicant has amended independent claims 1 and 7 to include the limitation turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the first memory section from being accessed. Additionally, claim 1 is amended to remove the step labels (a), (b) and (c), and claims 1 and 7 are amended to correct grammar by adding the additional word "on". No new matter is entered. In particular, refer to paragraph [37], stating, "Therefore, the data in the boot code section 62 is safe from being accessed, deleted, or updated incorrectly when the address translator 50 is turned on." Applicant notes that Kaiser et al. do not teach turning on the address translator for protecting a first memory section from being accessed. Instead, Kaiser et al. utilize the circuit of Figure 2 of Kaiser et al. to allow two microprocessors 108 and 109 to both access the IPL 105 even though they have different address bit lengths (microprocessor 108 = M-bit, microprocessor 109 = X-bit). Because Kaiser et al. do not teach or suggest turning on the address translator utilizing the control signal so that the second logic address data is outputted as the physical address data when it is required to protect the first memory section from being accessed, applicant asserts that the present invention as claimed

in currently amended claim 1 should not be found anticipated by Kaiser et al. A similar argument also applies to independent claim 7. As claims 2-6, and 7-21 are dependent on claims 1 and 7, if claims 1 and 7 are found allowable, so too should dependent claims 2-6 and 7-21. Further comments regarding the other amendments made to the claims and the patentability of specific dependent claims is provided below.

Claims 2, 5 and 6 are amended to remove the reference to Step (b) and to fix grammar by adding the word "on". No new matter is entered.

Claim 11 is additionally amended to fix grammar by adding the word "on". No new matter is entered.

New claims 14-21

New dependent claims 14 and 18 are added to claim the limitation that the operating unit of the address translator is an adder. No new matter is entered. In particular, refer to paragraph [34] stating, "the operating unit 54 of the address translator 50 is an adder". Applicant notes that such implementation is in contrast to Kaiser et al. because Kaiser et al. teach a concatenating circuit 203, not an adder. See col 4, lines 11-12. Consideration of claims 14 and 18 is respectfully requested.

New dependent claims 15 and 19 are added to claim the limitation that the memory section comprises boot code for a microprocessor. No new matter is entered. In particular, please refer to paragraph [23] stating, "… a non-volatile memory 60 including a boot code section 62". Claims 15 and 19 should be found allowable for at least the same reasons as provided above for independent claims 1 and 7. Consideration of claims 15 and 19 is respectfully requested.

New dependent claims 16 and 20 are added to claim the limitations turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when power is turned on or restored to the microprocessor to thereby allow access to the boot code; and when the microprocessor has successfully booted the system according to the boot code, turning on the address translator utilizing the control

signal so that the second logic address data is outputted as the physical address data to thereby protect the boot code from being accessed. No new matter is entered. In particular, please refer to paragraphs [45] and [46] of the specification teaching such operation. Applicant notes that Kaiser et al. do not teach or suggest such operation. That is, no mention of turning off the address translator at power on, or turning the address translator on after successfully booting the microprocessor is made by Kaiser at al. Consideration of claims 16 and 20 is respectfully requested.

New dependent claims 17 and 21 are added to claim the limitation turning off the address translator utilizing the control signal so that the first logic address data is outputted as the physical address data when it is required to erase or update the boot code to thereby allow access to the boot code in the first memory section by the microprocessor. No new matter is entered. In particular, please refer to paragraph [47] teaching such operation. Again, applicant points out that Kaiser et al. do not teach or suggest anything about how to erase or update the boot code in the IPL 105. Consideration of claims 17 and 21 is respectfully requested.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)